SOC Design Flow and Tools

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Project 1
Out: 10/22/2003
Due: 11/19/2003 for (a) and (b)
11/24/2003 for (c) and (d)

1. Project Purpose
This project intends to make you familiar with how to find a synthesizable IP and evaluate the quality of the IP core.

2. Works to Be Done
Go to the web site http://www.lug-kiel.de/links/details/hdl.html of Infos zu Open IP / Open Cores. Find a synthesizable IP core. Your are then asked to performed the following tasks:

(a). Verify whether the IP correctly perform its function. You have to explain in details how you verify it.
(b). Synthesize this IP into a gate level representation using TSMC 0.18 cell library.
(c). Place and route this IP using Cadence Silicon Ensemble tool sets.
(d). Perform post layout timing verification using Synopsys Prime time. Prior to doing verification you have to extract the RC delay (or capacitance) for each net from the layout.

Note that every student should have a different IP.

3. Report
You should write a report to describe your work and results. The format of the report is as follows:
1. Introduction
2. Methods
3. Results
4. Discussions