Rung-Bin Lin

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EXPERIENCE

2008-present	Professor, Department of Computer Science and Engineering, **Yuan Ze University**, Chung-Li, 320 Taiwan.
1995-2008	Associate Professor, Department of Computer Science and Engineering, **Yuan Ze University**, Chung-Li, 320 Taiwan.
1994-1995	Research Associate, Application and Research Center of Information Technology, **Tatung Institute of Technology**, Taipei.
1992-1994	Research and Development Staff, Large Scale Computing Division, **IBM**, Poughkeepsie, New York, USA.
1986-1987	Research Assistant, **ITRI**, Hsin-Chu, Taiwan.

EDUCATION

1987-1992	Ph.D. Computer and Information Science, University of Minnesota, Minneapolis, Minnesota, USA.
1980-1984	BS., Computer Engineering, National Chiao-Tung University, Hsin-Chu, Taiwan.

PROFESSIONAL ACTIVITIES

- Professional Societies
  - IEEE Member
  - IEICE Member
- Conference activities
  - IEEE/ACM Asia and South Pacific Design Automation Conference (ASPDAC), 2012, 2013, 2014
  - IEEE International Conference on Computer Design (ICCD) 2012, 2013.
  - ASPDAC session chair, 2013, 2014
  - ACM/IEEE GLSVLSI session chair, 2014
  - Technical program committee member, the 16th Workshop on Synthesis And System Integration of Mixed Information technologies (SASIMI), Taiwan, 2010
  - Technical program committee member, the 15th Workshop on Synthesis And System Integration of Mixed Information technologies (SASIMI), Japan, 2009
  - Session co-chair of International Symposium on VLSI Design, Automation and Test (VLSI-DAT), 2007
  - Workshop co-chair for International Workshop on Computer Architecture, VLSI, and Embedded Systems in conjunction with International Computer

Symposium, Taipei, Dec. 4-6, 2006

- Session chair and member of program committee of VLSI Design/CAD Symposium, annually held in Taiwan

- Reviewers of journals

  IEEE Transactions on VLSI Systems, IEEE Transactions on CAD, IEEE Transactions on Automation Science and Engineering, IEEE Transactions on Circuits and Systems, IET Proceedings Computer and Digital Techniques, IET Circuits, Devices & Systems, ACM TODEAS, Information Sciences, Integration (the VLSI Journal), International Journal of Computer Mathematics, Journal of Low Power Electronics, Journal of the Chinese Institute of Electrical Engineering, Journal of Information Science and Engineering, The Computer Journal, Computer and Electrical Engineering.

RESEARCH INTEREST

My research interest mainly focuses on the electronic design automation, especially on low-power designs, physical layout synthesis (partitioning, placement, and routing), structured ASIC, standard cell library, timing analysis, computer architecture, and VLSI design.

PUBLICATIONS

(A). Journals

[1] Hui-Hsiang Tung*, Rung-Bin Lin, Mei-Chen Li, and Tsung-Han Heish, "Standard Cell Like Via-Configurable Logic Blocks for Structured ASIC in an Industrial Design Flow," IEEE Transactions on VLSI Systems, Vol. 20, No. 12, pp. 2184-2197, Dec. 2012.

[2] Lung-Jen Lee*, Wang-Dauh Tseng, Rung-Bin Lin and Cheng-Ho Chang , "2n Pattern Run-Length for Test Data Compression," IEEE Transactions on CAD of Integrated Circuits and Systems, Vol. 31, No. 4, pp. 644-648, April 2012.

[3] Lung-Jen Lee*, Wang-Dauh Tseng, and Rung-Bin Lin, "Reduction of Test Data Volume and Test Application Time by Scan Chain Disabling Technique," Journal of Chinese Institute of Engineer, Vol. 35, No. 6, pp. 687-696, Sept. 2012.

[4] Lung-Jen Lee*, Wang-Dauh Tseng, and Rung-Bin Lin, "Mismatch Address Indexing For Test Data Compression," Journal of Chinese Institute of Engineer, 34:8, 1035-1045, Dec. 2011.

[5] Lung-Jen Lee*, Wang-Dauh Tseng, and Rung-Bin Lin, "An Internal Pattern Run-length Methodology for Slice Encoding," ETRI Journal, Vol. 33, No. 3, pp. 374-381, June 2011.

[6] Wang-Dauh Tseng*, Lung-Jen Lee, and Rung-Bin Lin, "Deterministic Built-in Self-Test Using Multiple Linear Feedback Shift Registers for Test Power and Test Volume Reduction," IET Computers & Digital Techniques, Vol. 4, No. 4, pp. 317-324, July 2010.

[7] Wang-Dauh Tseng, Lung-Jen Lee*, and Rung-Bin Lin, "Reduction of Power Dissipation During Scan Testing by Test Vector Ordering," Journal of Chinese Institute of Engineer, Vol. 33, No. 2, pp. 263-270, Mar. 2010.

[8] Rung-Bin Lin, "Inter-wire Coupling Reduction Analysis of Bus-Invert Coding," IEEE Transactions on Circuits and Systems I, Vol. 55, No. 7, 1911-1920, Aug. 2008.

[9] Rung-Bin Lin, “Variable-Sized Object Packing and Its Applications to Instruction Cache Design,” Computers & Electrical Engineering, Vol. 34, No. 5, Sept. pp. 438-444, 2008.

[10] Lung-Jen Lee, Wang-Dauh Tseng, and Rung-Bin Lin, “Power Reduction during Scan Testing based on Multiple Capture Technique,” IEICE Trans. on Electronics, Vol. E91-C,No.5, May, 2008.

[11] Meng-Chiou Wu and Rung-Bin Lin, “Finding Dicing Plans for Multiple Project Wafers Fabricated with Shuttle Mask,” Journal of Circuits, Systems, and Computers, Vol. 17, No. 1, pp. 15-31, Feb. 2008.

[12] Meng-Chiou Wu, Rung-Bin Lin, and Shih-Cheng Tsai, “Chip Placement in a Reticle for Multiple Project Wafer Fabrication,” ACM Transactions on Design Automation of Electronic Systems, Vol. 13, No. 1, Jan. 2008.

[13] Rung-Bin Lin, Meng-Chiou Wu, and Shih-Cheng Tsai, “Reticle Design for Minimizing Multiproject Wafer Production Cost,” IEEE Transactions on Automation Science and Engineering, vol. 4, no. 4, pp. 589-595, Oct. 2007.

[14] Rung-Bin Lin and Shu-Yu Chen, “Conjugate Conflict Continuation Graphs for Multi-layer Constrained Via Minimization,” Information Sciences: An International Journal, 177 (2007) 2436-2447.

[15] Rung-Bin Lin and Chi-Ming Tsai, “Theoretical Analysis of Bus-Invert Method,” IEEE Transactions on VLSI Systems, Vol. 10, No. 6, pp. 929-935, 2002.

[16] Rung-Bin Lin, “Comments on “Filling Algorithms and Analyses for Layout Density Control”,” IEEE Transactions on CAD, Vol. 21, No. 10, pp. 1209-1211, October 2002.

[17] Eric Q. Kang, Rung-Bin Lin and Eugene Shragowitz, “Fuzzy Logic Approach to VLSI Placement,” IEEE Transactions on Very Large Scale Integration Systems, VOL. 2, NO. 4, pp. 489-501, December 1994.

[18] Suphachai Sutanthavibul, Eugene Shragowitz and Rung-Bin Lin, “An Adaptive Timing-Driven Placement for High Performance VLSI's,” IEEE Transactions on Computer-Aided Design, VOL. 12, NO. 10, pp. 1488-1498, October 1993.

[19] Habib Youssef, Rung-Bin Lin and Eugene Shragowitz, “Bounds on Net Delays for VLSI Circuits,” IEEE Transactions on Circuits and Systems-II: Analog and Digital Signal Processing, VOL. 39, NO. 11, pp. 815-824, November 1992.

[20] Eugene Shragowitz and Rung-Bin Lin, “Combinatorial Optimization by Stochastic Automata,” Annals of Operations Research 22, pp. 293-324, 1990.

(B). International Conferences

[1] Ta-Kai Lin, Kuen-Wey Lin, Chang-Hao Chiu, Rung-Bin Lin, “Logic Block and Design Methodology for Via-configurable Structured ASIC using Dual Supply Voltages,” Great Lakes Symposium on VLSI (GLSVLSI), pp. 111-116, 2014.

[2] Chiung-Chih Ho, Hsin-Pei Tsai, Rung-Bin Lin, “Rover II: A Router for Via Configurable Structured ASIC with Standard Cells and IPs,” 18th Workshop on Synthesis and System Integration of Mixed Information Technologies (SASIMI), Sapporo, Japan, Oct. 2013.

[3] Ta-Kai Lin, Kuen-Wey Lin, Chang-Hao Chiu, Rung-Bin Lin, “Via-Configurable Structured ASIC using Dual Supply Voltages,” 18th Workshop on Synthesis and System Integration of Mixed Information Technologies (SASIMI), Sapporo, Japan, Oct. 2013.

[4] Hsin-Hung Liu, Rung-Bin Lin, and I-Lun Tseng, “Relocatable and resizable SRAM synthesis for via configurable structured ASIC,” ISQED, pp. 494-501,

2013.
[5] Tsung-Han Heish and Rung-Bin Lin, “Via-Configurable Structured ASIC Implementation of OpenRISC 1200 Based SoC Platform,” International Symposium on Next-Generation Electronics, Kaohsiung, Taiwan, 2013.
[6] Chia-Chieh Lu and Rung-Bin Lin, “Slack Budgeting and Slack to Length Converting for Multi-bit Flip-Flop Merging,” DATE, pp. 1837-1842, 2013.
[7] Yao-Ting Wu and Rung-Bin Lin, “Replacement of Flip-Flops by Latches and Pulsed Latches for Power and Timing Optimization,” 17th Workshop on Synthesis and System Integration of Mixed Information Technologies (SASIMI), Beppu, Oita, Japan, March 2012. (*Outstanding paper award*)
[8] Hsin-Pei Tsai, Rung-Bin Lin, and Liang-Chi Lai, “Design and Analysis of Via-Configurable Routing Fabrics for Structured ASICs,” DATE, pp. 1479 - 1482, 2012.
[9] Liang-Chi Lai, Hsih-Hang Chang, and Rung-Bin Lin, “Rover: Routing on Via-Configurable Fabrics for Standard-Cell-Like Structured ASICs,” GLSVLSI, pp. 37-42, 2011.
[10] Shih-Jung Hsu and Rung-Bin Lin, “Clock Gating Optimization with Delay-Matching,” DATE, pp. 1-6, 2011.
[11] Cheng-Ho Chang, Lung-Jen Lee, Wang-Dauh Tseng, and Rung-Bin Lin, “2n Pattern Run-Length for Test Data Compression,”International Computer Symposium (ICS), pp. 562 – 567, 2010.
[12] Cheng-Ho Chang, Lung-Jen Lee, Wang-Dauh Tseng, and Rung-Bin Lin, “Cascaded Broadcasting for Test Data Compression,” International Computer Symposium (ICS), pp. 557 – 561, 2010.
[13] Yu-Chen Chen, Hou-Yu Pang, Kuen-Wen Lin, Rung-Bin Lin, Hui-Hsiang Tung, Shih-Chieh Su, “Via Configurable Three-Input Lookup-Tables for Structured ASICs,” IEEE/ACM Great Lake Symposium on VLSI, pp. 49-54, 2010.
[14] I-Wei Lee, Wen-Hao Chen, and Rung-Bin Lin, “Clock Routing for Structured ASICs with Via-Configurable Fabrics,” International Symposium on Quality Electronic Design, pp. 777 - 784, March, 2010.
[15] Sin-Yu Chen, Rung-Bin Lin, Hui-Hsiang Tung, and Kuen-Wey Lin, “Power Gating Design for Standard-Cell-Like Structured ASICs,” DATE, pp. 514 - 519, March 2010.
[16] Hui-Hsiang Tung, Yu-Chen Chen, Da-Wei Hsu, Shih-Jung Hsu, Sin-Yu Chen, and Rung-Bin Lin, “Via-configurable Logic Block Architectures for Standard Cell like Structured ASICs,” The 12th International Symposium on Integrated Circuits, pp. 17-20, Dec. 14-16, Singapore, 2009. (Invited paper)
[17] Yu-Wen Tsai, Kun-Chen Wu, Hui-Hsiang Tung, and Rung-Bin Lin, “Using Structured ASIC to Improve Design Productivity,” The 12th International Symposium on Integrated Circuits, pp. 25-28, Dec. 14-16, Singapore, 2009.
[18] Po-Heng Chu, Rung-Bin Lin, Da-Wei Hsu, Yu-Hsing Chen, and Wei-Chih Tseng “Context-aware Post Routing Redundant Via Insertion,” IEEE Computer Society Annual Symposium on VLSI, pp. 37-42, 2009.
[19] Rung-Bin Lin, Tsung-Han Lin, and Shin-An Wu, “Circuit Acyclic Clustering with Input/Output Constraints and Applications,” International Symposium on VLSI Design, Automation, and Test, pp. 110-113, 2009.
[20] Lung-Jen Lee, Wang-Dauh Tseng, Rung-Bin Lin, and Chi-Wei Yu, “Deterministic Built-in Self-Test Using Multiple Linear Feedback Shift Registers for Low-Power

Scan Testing," IEEE Asian Test Symposium (ATS), pp.111-116, Nov. 2009.
[21] Lung-Jen Lee, Wang-Dauh Tseng, Rung-Bin Lin, and Chen-Lun Lee, "A Multi-Dimensional Pattern Run-Length Method for Test Data Compression,"IEEE Asian Test Symposium (ATS), pp. 325-330, Nov. 2009.
[22] Lung-Jen Lee, Wang-Dauh Tseng, Rung-Bin Lin, and Zheng-Yi Xie, "A Method of Don't-Care Bits Filling for Capture Power Reduction," International Conference on High-Speed Circuit Design, Section H3-1 Oct. 2009.
[23] Lung-Jen Lee, Wang-Dauh Tseng, Rung-Bin Lin, Cheng-Chi Yang, and Ying-Chung Lai, "A Run-length based Compression Method for Multiple-Scan testing,"International Conference on High-Speed Circuit Design, Section H3-2 Oct. 2009.
[24] Lung-Jen Lee, Wang-Dauh Tseng, Rung-Bin Lin, Cheng-Chi Yang, and Ying-Chung Lai, "Segmented LFSR for Deterministic Test Generations," International Conference on High-Speed Circuit Design, Section H3-2 Oct. 2009.
[25] Wei-Chih Tseng, Yu-Hsing Chen, Rung-Bin Lin, "Router and Cell Library Co-development for Improving Redundant Via Insertion at Pins," IEEE International Conference on Computer Design, pp. 646-651, 2008.
[26] Mei-Chen Li, Hui-Hsiang Tung, Chien-Chung Lai, and Rung-Bin Lin, "Standard cell like via-configurable logic block for structured ASICs," IEEE Computer Society Annual Symposium on VLSI, pp. 381 – 386, 2008.
[27] Rung-Bin Lin, Da-Wei Hsu, Ming-Hsine Kuo, and Meng-Chiou Wu, "Reticle Exposure Plans for Multi-Project Wafers," IEEE Workshop on Design and Diagnostics of Electronic Circuits and Systems, pp. 1-4, 2007.
[28] Sungjae Kim, Eugene Shragowitz, George Karypis, and Rung-Bin Lin, "Interleaving of Gate Sizing and Constructive Placement for Predictable Performance," International Symposium on VLSI Design, Automation, and Test, pp. 1-4, 2007.
[29] Tsai-Ying Lin, Tsung-Han Lin, Hui-Hsiang Tung, Rung-Bin Lin, "Double-Via-Driven Standard Cell Library Design" International Conference on Design, Automation, and Test in Europe, pp. 1-6, 2007.
[30] Ming-Hsine Kuo, Meng-Chiou Wu, Rung-Bin Lin, "Sensitivity Analysis of Multi-project Wafers Production Cost," In the Proc. of Workshop on Computer Architecture, VLSI, and Embedded Systems, International Computer Symposium, Taipei, 2006.
[31] Lung-Jen Lee and Rung-Bin Lin, "Using Essential Inverters for Interconnect Delay Reduction," In the Proc. of Workshop on Computer Architecture, VLSI, and Embedded Systems, International Computer Symposium, Taipei, 2006.
[32] Hsun-Chieh Yu and Rung-Bin Lin, "Is More Redundancy Better for On-Chip Bus Encoding," IEEE International Symposium on Circuits and Systems, pp. 2209-2212, 2006.
[33] Meng-Chiou Wu, and Shr-Cheng Tsai, and Rung-Bin Lin, "Floorplanning Multiple Reticles for Multi-project Wafers," International Symposium on VLSI Design, Automation, and Test, pp. 143-146, 2006.
[34] Rung-Bin Lin, Meng-Chiou Wu, Wei-Chiu Tseng, Ming-Hsine Kuo, Tsai-Ying Lin, and Shr-Cheng Tsai, "Design Space Exploration for Minimizing Multi-Project Wafer Production Cost, "The 11th Asia and South Pacific Design Automation Conference, pp. 783-788, 2006.
[35] Meng-Chiou Wu and Rung-Bin Lin, "Reticle Floorplanning of Flexible Chips for Multi-project Wafers," IEEE/ACM Great Lake Symposium on VLSI, pp.

494-497, 2005.
[36] Meng-Chiou Wu and Rung-Bin Lin, “Reticle Floorplanning and Wafer Dicing for Multiple Project Wafers,” International Symposium on Quality Electronic Design, pp. 610-615, 2005.
[37] Meng-Chiou Wu and Rung-Bin Lin, “Multiple Project Wafers for Medium-Volume IC Production,” IEEE International Symposium on Circuits and Systems, pp. 4725-4728, 2005.
[38] Meng-Chiou Wu and Rung-Bin Lin, “A Comparative Study on Dicing of Multiple Project Wafers,” IEEE Computer Society Annual Symposium on VLSI, pp. 314-315, 2005.
[39] Guang-Wan Liao, Ja-Shong Feng, and Rung-Bin Lin, “A Divide-and-Conquer Approach to Estimating Minimum/Maximum Leakage Current,” IEEE International Symposium on Circuits and Systems, pp. 4717-4720, 2005.
[40] Rung-Bin Lin, “Coupling Reduction Analysis of Bus-Invert Coding,” IEEE International Symposium on Circuits and Systems, pp. 5862-5865, 2005.
[41] Rung-Bin Lin and Shu-Yu Chen, “Multi-layer Constrained Via Minimization with Conjugate Conflict Continuation Graphs,” IEEE International Symposium on Circuits and Systems, pp. 525-528, 2004.
[42] Chi-Ming Tsai, Guang-Wan Liao, and Rung-Bin Lin, “A Low Power-Delay Product Page-Based Address Bus Coding Method,” Proceedings of the 16th International Conference on VLSI Design, pp. 521-526, 2003.
[43] Chi-Ming Tsai, Kun-Tien Kuo, Chyi-Hui Hong, and Rung-Bin Lin, “An Adaptive Interconnect-Length Driven Placer,” Proceedings of the 7th Asia and South Pacific Design Automation Conference and 15th International Conference on VLSI Design, pp. 393-398, Jan., 2002.
[44] Rung-Bin Lin and Chi-Ming Tsai, “Weight-Based Bus-Invert Coding for Low-Power Applications,” Proceedings of the 7th Asia and South Pacific Design Automation Conference and 15th International Conference on VLSI Design, pp. 121-125, Jan., 2002.
[45] Chi-Ming Tsai, Tsai-Min Chiang, Chyi-Hui Hong, Kun-Tien Kuo, and Rung-Bin Lin, “A Low Power-delay-product Multiplier with Dynamic Operand Exchange,” IEEE Asia Pacific Conference on Circuits and Systems, pp. 501-504, December 2000.
[46] Rung-Bin Lin and Chi-Ming Tsai, “Theoretical Analysis of Bus-Invert Coding,” The Proceedings of the IEEE 43rd Midwest Symposium on Circuits and Systems, pp., 742-745, August 2000.
[47] Rung-Bin Lin and Jing-Chang Chen, “Low Power CMOS Off-Chip Drivers with Slew-rate Difference,” The Proceedings of IEEE Asia and South Pacific Design Automation Conference, Hong Kong, pp. 169-172, January 1999.
[48] Rung-Bin Lin, Isaac Shuo-Hsiu Chou and Chi-Ming Tsai, “Benchmark Circuits Improve the Quality of a Standard Cell Library,” the proceedings of IEEE Asia and South Pacific Design Automation Conference, Hong Kong, pp. 173-176, January 1999.
[49] Rung-Bin Lin, Sung-Ming Su, and Chi-Ming Tsai, “Formulas for Computation of Transition Density for Power Estimation,” Proceedings of International Conference on Computer Systems Technology for Industrial Applications-Chip Technology, Hsinchu, R.O.C., pp. 212-218, April 1998.
[50] Chi-Ming Tsai, Jinq-Chang Chen, Issac Shuo-Hsiu Chou, Shu-Ren Ker, Jiunn-Ren Chen, Hui-Hsiang Tung, Tsai-Min Chiang, Chyi-Bin Lin, Rung-Bin

Lin, and Yin-Kuan Lin, “Development of a 0.25um CMOS Standard Cell Library,” Proceedings of International Conference on Computer Systems Technology for Industrial Applications-Chip Technology, Hsinchu, R.O.C., pp. 73-78, April 1998.

[51] Rung-Bin Lin and Meng-Chiou Wu, “A New Statistical Approach to Timing Analysis of VLSI Circuits,” Proceedings of the 11th International Conference on VLSI Design, Chennai, India, pp. 507-513, January 1998.

[52] Rung-Bin Lin and Chi-Ming Tsai, “Analytical Study of Performance Evaluation for x86 Instructions to Micro-ops Decoder,” Proceedings of International Conference on Computer Architecture, International Computer Symposium, R.O.C., pp. 113-120, December 1996.

[53] Rung-Bin Lin and Eugene Shragowitz, “Fuzzy Logic Approach to Placement Problem,” Proceedings of the 29th ACM/IEEE Design Automation Conference, pp. 153-158, June 1992.

[54] Habib Youssef, Rung-Bin Lin and Eugene Shragowitz, “Bounds on Net Delay for Physical Design of Fast Circuits,” Proceedings of IFIP TC 10/WG 10.5, 1991 International Conference on VLSI, pp. 111-118.

[55] Eugene Shragowitz and Rung-Bin Lin, “Combinatorial Optimization, Markov Chains and Stochastic Automata,” The first International Conference on Numerical Solution of Markov Chains, pp. 582-602, 1990.

(c). Domestic Conferences

[1] Yao-Ting Wu, Rung-Bin Lin, “Study of Pulse Width for Pulse Latches,” Proceedings of the 22nd VLSI Design/CAD Symposium, Taiwan, 2012.

[2] Jian Zeng, Rung-Bin Lin, Jian-Yang Zhou, Yi-Yu Liu, “Transition Inversion Coding with Parity Check for Off-Chip Serial Transmission,” Proceedings of the 22nd VLSI Design/CAD Symposium, Taiwan, pp. 88-91, 2012.

[3] Rung-Bin Lin, “On the Applications of Partition Diagrams for Integer Partitioning,” The 23rd Workshop on Combinatorial Mathematics and Computational Theory, Chang Hua, 2006.

[4] Rung-Bin Lin, “Efficient Data Structures for Storing the Partitions of Integers,” The 22rd Workshop on Combinatorial Mathematics and Computational Theory, Tainan, 2005.

[5] Jia-Xun Yang and Rung-Bin Lin, “Wire Width Sizing for Delay and Yield Optimization,” Proceedings of the 16th VLSI Design/CAD Symposium, Taiwan, 2005.

[6] Rung-Bin Lin, “Clique Modeling of Hyperedges for Circuit Partitioning,” Proceedings of the 14th VLSI Design/CAD Symposium, Taiwan, 2003.

[7] Rung-Bin Lin and Jen-Yan Shiu, “Generation of Synthetic Circuits for CAD Tool Development,” Proceedings of the 13th VLSI Design/CAD Symposium, Taiwan, pp. 88-91, 2002.

[8] Meng-Chiou Wu and Rung-Bin Lin, “Timing Failure Analysis of VLSI Circuits by Extreme Value Distribution,” Proceedings of the 10th VLSI Design/CAD Symposium, pp. 95-98, Nan-Tou, Taiwan, August 1999.

[9] Chi-Ming Tsai and Rung-Bin Lin, “Designing of a CMOS Standard Cell Library,” Proc. of Microprocessor Symposium, pp. 41-46, Hsinchu, May 1999.

[10] Rung-Bin Lin, “Basic CMOS Standard Cell Library Design,” Proc. of Microprocessor Symposium, pp. 47-50, Hsinchu, May 1999.

[11] Chi-Ming Tsai and Rung-Bin Lin, “On the Study of Intel P6-Like Decoders,” Proceedings of National Computer Symposium, pp. C51-C56, R.O.C., December 1997.

[12] Rung-Bin Lin and Shu-Ren Ker, “An Automatic Library Development System,” The 8th VLSI Design/CAD Symposium, Sun-Moon Lake, R.O.C., pp. 237-240, August 1997.

(D). Book Chapters

[1] Eugene Shragowitz and Rung-Bin Lin, "Combinatorial Optimization, Markov Chains and Stochastic Automata," Chapter 29 in the book "Numerical Solution of Markov Chains," Edited by William J. Stewart. Marcel Dekker, Inc, New York, 1991.

[2] Rung-Bin Lin, Meng-Chiou Wu, Shih-Cheng Tsai, and Da-Wei Hsu, "Reticle Floorplanning and Simulated Wafer Dicing for Multiple-Project Wafers by Simulated Annealing", Chapter 13 in the book "Simulated Annealing", ISBN 978-3-902613-33-2, Edited by Cher Ming Tan, published by In-Teh, Vienna, Austria, Sept. 2008.

(E). Patents

[1] WAFER LITHOGRAPHIC MASK AND WAFER LITHOGRAPHY METHOD USING THE SAME, by Rung-Bin Lin and Shih-Cheng Tsai, USA patent, Patent No. US 7,838,175 B2.

[2] 晶圓微影遮罩、晶圓微影裝置及其晶圓微影方法, 蔡士成, 林榮彬, Taiwan patent, 發明第 I 331699 號.