Project 1: Circuit properties of MOS transistors

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Purpose:
This project is to make students becoming familiar with the properties of MOS transistors and the usage of SPICE.

Introduction:
There are two types of MOS transistors, pMOS and nMOS, which are usually employed as digital switches to implement some Boolean functions. Although the MOS transistors are treated conceptually as digital devices that have logical values either “true” or “false”, they are intrinsically analog devices whose node voltage and branch current are real numbers. Thus, in order to make best use of these transistors, one has to understand the basic circuit properties of these transistors. These basic circuit properties depict the relationship between inputs and outputs in terms of branch current and node voltage and are governed by the materials used and the physical structure created to form the MOS transistors. Generally, the relationship between input and output can be specified by some equations like those found in the majority of textbooks. Alternatively, their relationship can be obtained by circuit simulation. The most often used tool for circuit simulation is called SPICE (Simulation Program with Integrated Circuit Emphasis). SPICE was designed in the early of 1970s at the University of California at Berkeley. Although it was originally used with emphasis to simulate the behavior of integrated circuits, it is general enough to simulate analog circuits. In fact, it has become an industry standard for analog simulation. More technical details about SPICE can be found in many books, while a history about SPICE can be found in [1].

MOS transistors are four-terminal devices: source, drain, gate and substrate. The gate controls whether a current flow between source and drain can be established. Source and drain are physically equivalent and their name assignment depends on the direction of current flow. Substrate acts as the fourth terminal. A pMOS transistor has a negatively doped substrate while an nMOS transistor has a positively doped
substrate. The current flow between source and drain is mainly formed by the movement of majority carriers which are electrons for an \textit{nMOS} transistor and holes for a \textit{pMOS} transistor. The terminal supplying the majority carrier is called “source,” while the terminal receiving the majority carriers is called “drain.” In general, there is no other conducting path in a MOS transistor except the path between source and drain; that is there is no conducting path between source and gate, drain and gate, substrate and gate, substrate and source, or substrate and drain. Figure 1.1 depicts the structures of a \textit{pMOS} and \textit{nMOS} transistors.

Figure 1.1 Transistor structure.

When the gate voltage exceeding a threshold voltage $V_{th}$ ($V_{gs}$) for an \textit{nMOS} (\textit{pMOS}) transistor, the transistor starts to conduct and there is a significant current flow between its source and drain. Let $V_{gs}$ denote the voltage between the gate and the source, $V_{ds}$ and $I_{ds}$ denote respectively the voltage and current between its drain and source, $V_{dd}$ denote the power supply, and $V_{ss}$ denote the ground. In general, an \textit{nMOS}
transistor starts to conduct (i.e., $I_{ds}>0$) when $V_{gs}>V_{th}>0$, while a $pMOS$ transistor starts to conduct (i.e., $I_{ds}<0$) when $V_{gs}<V_{th}<0$. The transistors of this sort are called enhanced-mode transistors. When an $nMOS$ transistor is treated as a digital switch, if its gate voltage is equal to $V_{dd}$, the transistor is “ON” and $I_{ds}>0$, but if the gate is grounded, the transistor is “OFF” and $I_{ds}=0$. When a $pMOS$ transistor is treated as a digital switch, if its gate voltage is equal to $V_{dd}$, the transistor is “OFF” and $I_{ds}=0$, but if its gate is grounded, the transistor is “ON” and $I_{ds}<0$. However, one has to note that a transistor is “ON” or “OFF” not just when its gate voltage is at a certain values; instead, the transistor is “ON” or “OFF” within a range of voltage value. For an $nMOS$ transistor, it allows a good “0” (a bad “1”) to pass from its input to output; that is if the input is a good “0” (a good “1”), when the transistor is “ON”, a good “0” (a bad “1”) will appear at the output. On the contrary, for a $pMOS$ transistor, it allows a good “1” (a bad “0”) to pass from its input (source) to output (drain); that is, if the input is a good “1” (a good “0”), when the transistor is “ON”, a good “1” (a bad “0”) appears at the output. A good “1” is a voltage equal to $V_{dd}$, while a bad “1” is a voltage smaller than $V_{dd}$ but still treated as a logical “1”. Similarly, a good “0” is a voltage equal to 0, while a bad “0” is a voltage greater than 0 but still treated as a logical “0”. A switch combining a $pMOS$ and $nMOS$ transistors as shown in Figure 1.2 is called a transmission gate which allows a good “1” and a good “0” to pass completely. Table 1.1 shows some information for $nMOS$ and $pMOS$ transistors.

![Figure 1.2 A transmission gate.](image)
Table 1.1. Characteristics of nMOS and pMOS transistors

<table>
<thead>
<tr>
<th>Attributes</th>
<th>nMOS</th>
<th>pMOS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Majority carriers</td>
<td>Electrons</td>
<td>Holes</td>
</tr>
<tr>
<td>Mobility of majority carriers (typical value</td>
<td>500 cm²/V-sec</td>
<td>180 cm²/V-sec</td>
</tr>
<tr>
<td>for 1 um process)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Substrate doping (light)</td>
<td>p⁺</td>
<td>n⁺</td>
</tr>
<tr>
<td>Source/drain doping (heavy)</td>
<td>n⁺</td>
<td>p⁺</td>
</tr>
<tr>
<td>Substrate(well) contact doping (heavy)</td>
<td>n⁺</td>
<td>n⁺</td>
</tr>
<tr>
<td>Substrate(well) contact connection</td>
<td>Vss</td>
<td>Vdd</td>
</tr>
<tr>
<td>Threshold voltage(Enhanced mode)</td>
<td>Vtn&gt;0</td>
<td>Vtp&lt;0</td>
</tr>
<tr>
<td>Logic value of the gate to turn on transistor</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>Capability of passing logic value</td>
<td>poor 1, good 0</td>
<td>good 1, poor 1</td>
</tr>
</tbody>
</table>

Problem descriptions:

1. Use HSPICE to find out the \( I_{ds} \) of a pMOS transistor with gate length 0.35 um and width 1.2um in terms of \( V_{ds} \) decreasing from 0V to \(-V_{dd}=-3.3V\) respectively for \( V_{gs}=0V, -0.7V, -1.4V, -2.0V, -2.7V \) and \(-3.3V\). Can you find out a line similar to the one in Figure 2.9 of the textbook by Weste?

2. Perform a similar task for an nMOS transistor with gate length 0.35 um and width 1.2um. Note that \( V_{ds} \) should be increased from 0V to 3.3V respectively for \( V_{gs}=0V, 0.7V, 1.4V, 2.0V, 2.7V \) and 3.3V. Compare also the maximal current for each individual \( V_{gs} \) to that obtained for a pMOS transistor.

3. Take the transistor from problem 1 and connect a capacitor \( C_{load}=0.1\)PF to either its source or drain as shown in the following figure. Initially, completely discharge the capacitor and set the gate \( S \) to \( V_{dd}=3.3V \) and the input \( V_{in} \) to \( V_{dd} \). Then, change the gate \( S \) from \( V_{dd} \) to 0V within 1ns and observe the voltage change of \( V_{out} \) for the next 5ns. Is \( V_{in} \) equal to \( V_{out} \)? Next, change the input \( V_{in} \) from \( V_{dd} \) to 0V within 1ns and observe the voltage of \( V_{out} \) for the next 5ns. Is \( V_{out} \) equal to \( V_{in} \)?

![Diagram of circuit with transistor and capacitor](attachment:image.png)
4. Take the transistor from problem 2 and connect a capacitor $C_{load}=0.1\text{PF}$ to either its source or drain as shown in the following figure. Initially, completely discharge the capacitor and set the gate $S$ to the ground, and the input $V_{in}$ to $V_{dd}$. Then, change the gate $S$ from 0V from $V_{dd}$ within 1ns and observe the voltage change of $V_{out}$ for the next 5ns. Is $V_{out}$ equal to $V_{in}$? Next, change the input $V_{in}$ from $V_{dd}$ to 0V within 1ns and observe the voltage of $V_{out}$ for the next 5ns. Is $V_{out}$ equal to $V_{in}$?

![Diagram](image)

5. Combine the transistors respectively described in the problems 1 and 2 with a load $C_{load}=0.1\text{PF}$ as shown in the following figure. Initially, completely discharge the capacitor and set the gate $S$ to the ground, and the input $V_{in}$ to $V_{dd}$. Then, change the gate $S$ from 0V from $V_{dd}$ within 1ns and observe the voltage change of $V_{out}$ for the next 5ns. Is $V_{out}$ equal to $V_{in}$? Next, change the input $V_{in}$ from $V_{dd}$ to 0V within 1ns and observe the voltage of $V_{out}$ for the next 5ns. Is $V_{out}$ equal to $V_{in}$?

![Diagram](image)

6. What conclusion can you draw from the observations on the problems 3, 4 and 5?

**Notes:**

♥ A tutorial on how to login and use the computer system to do your work will also be posted on this web directory.

♥ This project will be due on April 9, 2001. Your report should include the simulation waveforms that give you the answers for the problems. You should also clearly identify which portion of waveforms gives you the answer.

**References:**

